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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,478	08/13/2001	Warren M. Farnworth	3401.5US (97-710.5)	7943

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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/928,478	FARI NORTH ET AL.
	Examiner	Art Unit
	John B. Vigushin	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-14 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,12,14,16-21* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ___ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed February 10, 2003 (Certificate of Mailing date: February 04, 2003). The Examiner acknowledges the amendments to Claims 1-4, 6-9, 11, 12, 16, 18, 19 and 21, and the cancellation of Claims 10 and 15. Accordingly, Claims 1-9, 11-14 and 16-21 remain pending in the instant amended Application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2-4 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2-4 recites the limitation ""said semiconductor die" in lines 2-3 of Claim 2 and line 2 of Claim 4. There is insufficient antecedent basis for this limitation in the claim. The rejection may be overcome by amending the base Claim 1 such that "device" is changed to --die-- in line 2 of Claim 1, which is clearly the intent of the Applicant as set forth in the paragraph of *Remarks* bridging pp.5-6 of Applicant's above-cited Amendment.

Claim 21 recites the limitation "the semiconductor device" in line 3. There is insufficient antecedent basis for this limitation in the claim. The rejection may be overcome by changing "device" to --die-- in line 3 of the claim.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. *Examiner's Note*: In the obviousness-type rejections that appear below, those rejections based on the US Patents in view of prior art relied upon the following prior art references:

Yunoki et al. (US 5,236,372)* Akram et al. (US 6,072,236)*

*Already made of the record in the instant Application.

6. Claims 1, 7, 8 and 11, and Claims 12, 16, 17, 19, 20, are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 15-16, 24-25 and 32-33 of U.S. Patent No. 6,144,560. Although the conflicting claims are not identical, and *since it is clearly the intent of the Applicant that "device" in line 2 of the instant amended Application Claim 1 should be --die-- (see the paragraph of Remarks bridging pp.5-6 of Applicant's above-cited Amendment),* they are not patentably distinct from each other:

Although the conflicting claims are not identical, they are not patentably distinct from each other because a comparison of the instant Application Claims 1, 7, 8 and 11 to patented Claims 15-16, 24-25 and 32-33 reveal that the Application Claims 1, 7, 8 and 11 define a generic embodiment of the species covered by patented Claims 15-16, 24-25 and 32-33. Accordingly, generic Application Claims 1, 7, 8 and 11 are anticipated by the patented species Claims 15-16, 24-25 and 32-33 and therefore preclude issuance of Application Claims 1, 7, 8 and 11 in accordance with *In re Goodman*, 29 USPQ2d 2010 (CAFC 1993). In other words, patented Claims 15-16, 24-25 and 32-33 already cover--i.e., "read on"--Application Claims 1, 7, 8 and 11. This is essentially the epitome of obviousness since the Application Claims 1, 7, 8 and 11 are not "in any way unobvious" over the patented Claims 15-16, 24-25 and 32-33.

Furthermore, patented Claims 15-16 recite a "substantially bare semiconductor device" and patented Claims 24-25 and 32-33 recite "a semiconductor device," comprising: in Claims 15-16 (see base Claim 9), "an active surface with a plurality of bond pads disposed along an edge thereof," and in Claims 24-25 and 32-33 (see base Claims 17 and 29), "an active surface, a bottom edge, at least one bond pad disposed proximate said bottom edge....". Application Claims 1, 7, 8 and 11 recite "[a] semiconductor device, comprising: at least one bond pad on a surface of a semiconductor device adjacent an edge thereof." The Examiner notes that "a semiconductor die" of Application Claims 1, 7, 8 and 11 is recognized in the art as a semiconductor device, or bare semiconductor device, comprising an active surface, as in patented Claims 15-16, 24-25 and 32-33, and therefore the "semiconductor die" of

Application Claims 1, 7, 8 and 11 is anticipated by patented Claims 15-16, 24-25 and 32-33.

For reasons similar to those cited above for instant Application Claims 1, 7, 8 and 11, the instant Application Claims 12 and 16, as well as additional Application Claims 17, 19 and 20 whose limitations are already covered by patented Claims 15-16, 24-25 and 32-33, also define a generic embodiment of the species covered by patented species Claims 15-16, 24-25 and 32-33 and, accordingly, are anticipated by the patented species Claims 15-16, 24-25 and 32-33 and therefore may not be issued in accordance with *In re Goodman*, as cited above.

7. Claims 4, 6 and 21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 15, 24 and 32 of U.S. Patent No. 6,144,560 in view of Yunoki et al.

Application Claim 4 discloses that the notch is tapered from a surface of the layer toward the surface of the die. Patented Claims 15, 24 and 32 do not teach this tapered feature of the notch. Yunoki et al. analogously teaches a circuit board device 30 for insertion into a connector 10 (Fig. 4), wherein the circuit board has a dielectric layer 34 with notches 35 located along the edge exposing circuit board terminals 32 (Fig. 2), said notches 35 being tapered (tapered portions shown at 35a) from a surface of the layer 34 toward the surface of the circuit board 30 in order to facilitate guiding the connector contacts 22 toward the exposed circuit board terminals 32 (Fig. 2; col.5: 63-col.6: 9). Since the analogous circuit board of Yunoki et al. and the semiconductor die of patented Claims 15, 24 and 32 share the same structural features suitable for insertion into a

connector body, as taught by Yunoki et al., then the use of tapered notches for facilitating insertion and reliable connection to the connector 10 of Yunoki et al. would have been readily recognized for use in the semiconductor die structure of patented Claims 15, 24 and 32. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to taper the notches in patented Claims 15, 24 and 32, as taught by Yunoki et al. and required by Application Claim 4, in order to facilitate insertion and reliable connection to a connector, as taught by Yunoki et al.

Application Claims 6 and 21 disclose that the notch substantially surrounds the at least one corresponding bond pad. Claims 15, 24 and 32 disclose that the notch exposes the bond pads through the polymer layer but do not teach the structural relationship between each notch and corresponding die bond claimed in Application Claim 6. Yunoki et al. analogously teaches a circuit board device 30 for insertion into a connector 10 (Fig. 4), wherein the circuit board has a dielectric layer 34 with notches 35 located along the edge that substantially surround the corresponding circuit board bond pads 32 in order to expose the bond pads 32 to the outside (Fig. 2), the dielectric layer 34 covering and inherently protecting the remaining portion of the connection surface 31 of circuit board 30 (col.5: 23-27). Since the analogous circuit board Yunoki et al. and the semiconductor active surface of Claims 15, 24 and 32 both have a layer of insulating material for protection of the circuitry on the active surface, then substantially surrounding the bond pads with the notches in the insulating material, taught by Yunoki et al., would have been readily recognized in the art of patented Claims 15, 24 and 32 in order to protect as much of the active surface circuitry as possible, exposing only the

bond pads required for external contact. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the polymer notch structures in patented Claims 15, 24 and 32 to substantially surround the at least one corresponding bond pad, as taught by Yunoki et al. and required by Application Claims 6 and 21, in order to maximize the protection of the active surface circuitry, as taught in the analogous circuit board art of Yunoki et al.

8. Application Claims 5 and 18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 15, 24 and 32 of U.S. Patent No. 6,144,560 in view of Akram et al.

Patented Claims 15, 24 and 32 teach all the elements of Application Claims 5 and 18 including that the polymer layer covers at least a portion of the active surface (the active surface, *generally*, in patent Claim 24; and the portion of the active surface *proximate* the semiconductor edge in patent Claims 15 and 32). Patented Claims 15, 24 and 32 do not teach that the polymer layer covers *substantially all* of the semiconductor active surface. Akram et al. teaches a semiconductor die 12 comprising a ceramic layer 20 (col.5: 47-51), the layer 20 having a notch 22 proximate the edge that exposes contact pads 116 (Figs. 6 and 7) and that covers all the remaining active die surface (i.e., covers "substantially all" of the active die surface) in order to protect the active surface circuitry from environmental contaminants. Since patented Claims 15, 24 and 32 and Akram et al. are in the same art of mounting semiconductor die in electronic packages, then the protection of the active die surface would have been readily recognized in the pertinent art of patented Claims 15, 24 and 32. Therefore, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to protect the active surface circuitry by modifying the polymer layer in patented Claims 15, 24 and 32 to cover substantially all of the active surface except the bond pads, as taught by Akram et al., in order to ensure device reliability and longevity.

9. Application Claim 9 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 15, 24 and 32 of U.S. Patent No. 6,144,560 in view of Yunoki et al.

Application Claim 9 requires that the polymer layer includes regions extending laterally between adjacent bond pads of the at least some bond pads. Claims 15, 24 and 32 disclose that the polymer layer has notches in the layer that expose the active surface bond pads but do not teach that the polymer layer includes regions extending laterally between adjacent bond pads of the at least some bond pads claimed in Application Claim 9. Yunoki et al. analogously teaches a circuit board device 30 for insertion into a connector 10 (Fig. 4), wherein the circuit board has a dielectric layer 34 with notches 35 located along the edge that substantially surround the corresponding circuit board bond pads 32 such that the layer includes regions extending laterally between adjacent bond pads 32 of at least some of the bond pads 32 (Fig. 2), said regions providing protection for the insertion portion of the active surface of the circuit board (col.5: 23-27). Since the analogous circuit board Yunoki et al. and the semiconductor active surface of Claims 15, 24 and 32 both have a layer of insulating material for protection of the circuitry on the active surface, then providing regions of an insulating layer extending laterally between adjacent bond pads of at least some of the

bond pads, as taught by Yunoki et al., would have been readily recognized in the art of patented Claims 15, 24 and 32 in order to protect as much of the active surface circuitry as possible and protecting the active surface proximate the edge when mounted. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the polymer layer in patented Claims 15, 24 and 32 such that the layer includes regions extending laterally between adjacent bond pads of the at least some bond pads in order to protect as much of the active surface circuitry as possible, especially the active surface proximate the edge when mounted, as taught in the analogous circuit board art of Yunoki et al.

10. Claim 14 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 15, 24 and 32 of U.S. Patent No. 6,144,560 in view of Yunoki et al.

Application Claim 14 requires that at least one edge of the at least one notch is beveled. Patented Claims 15, 24 and 32 do not teach this beveled feature of at least one edge of the at least one notch. Yunoki et al. analogously teaches a circuit board device 30 for insertion into a connector 10 (Fig. 4), wherein the circuit board has a dielectric layer 34 with notches 35 located along the edge exposing circuit board terminals 32 (Fig. 2), said notches 35 being beveled at the inner lateral edges of the notch (beveled portions shown at 35a) in order to facilitate guiding the connector contacts 22 toward the exposed circuit board terminals 32 (Fig. 2; col.5: 63-col.6: 9). Since the analogous circuit board of Yunoki et al. and the semiconductor die of patented Claims 15, 24 and 32 share the same structural features suitable for insertion into a

connector body, as taught by Yunoki et al., then the use of beveled notches for facilitating insertion and reliable connection to the connector 10 of Yunoki et al. would have been readily recognized for use in the semiconductor die structure of patented Claims 15, 24 and 32. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to bevel the notches in patented Claims 15, 24 and 32, as taught by Yunoki et al. and required by Application Claim 14, in order to facilitate insertion and reliable connection to a connector, as taught by Yunoki et al.

11. Claims 1, 7, 8 and 11, and Claims 12 and 16, are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 9-10, 17-18, 26-27 and 34-35 of U.S. Patent No. 6,295,209 B1. Although the conflicting claims are not identical, and *since it is clearly the intent of the Applicant that "device" in line 2 of the instant amended Application Claim 1 should be --die-- (see the paragraph of Remarks bridging pp.5-6 of Applicant's above-cited Amendment),* they are not patentably distinct from each other:

Although the conflicting claims are not identical, they are not patentably distinct from each other because a comparison of the instant Application Claims 1, 7, 8 and 11 to patented Claims 9-10, 17-18, 26-27 and 34-35 reveal that the Application Claims 1, 7, 8 and 11 define a generic embodiment of the species covered by patented Claims 9-10, 17-18, 26-27 and 34-35. Accordingly, generic Application Claims 1, 7, 8 and 11 are anticipated by the patented species Claims 9-10, 17-18, 26-27 and 34-35 and therefore preclude issuance of Application Claims 1, 7, 8 and 11 in accordance with *In re Goodman*, 29 USPQ2d 2010 (CAFC 1993). In other words, patented Claims 9-10, 17-

18, 26-27 and 34-35 already cover--i.e., "read on"--Application Claims 1, 7, 8 and 11. This is essentially the epitome of obviousness since the Application Claims 1, 7, 8 and 11 are not "in any way unobvious" over the patented Claims 9-10, 17-18, 26-27 and 34-35.

Furthermore, patented Claims 9-10, 17-18, 26-27 and 34-35 recite "a semiconductor device," comprising: in Claims 9-10 (see base Claim 1), "an active surface with a plurality of bond pads disposed proximate an edge thereof," in Claims 17-18 (see base Claim 11), "an active surface with a plurality of bond pads disposed along an edge thereof," in Claims 26-27 and 34-35 (see base Claims 19 and 31) "an active surface, an edge, at least one bond pad disposed proximate said edge....". Application Claims 1, 7, 8 and 11 recite "[a] semiconductor device, comprising: at least one bond pad on a surface of a semiconductor device adjacent an edge thereof." The Examiner notes that "a semiconductor die" of Application Claims 1, 7, 8 and 11 is recognized in the art as a semiconductor device comprising an active surface, as in patented Claims 9-10, 17-18, 26-27 and 34-35, and therefore the "semiconductor die" of Application Claims 1, 7, 8 and 11 is anticipated by patented Claims 9-10, 17-18, 26-27 and 34-35.

For reasons similar to those cited above for instant Application Claims 1, 7, 8 and 11, the instant Application Claims 12 and 16, as well as additional Application Claims 17, 19 and 20 whose limitations are already covered by patented Claims 9-10, 17-18, 26-27 and 34-35, also define a generic embodiment of the species covered by patented species Claims 9-10, 17-18, 26-27 and 34-35 and, accordingly, are anticipated by the

patented species Claims 9-10, 17-18, 26-27 and 34-35 and therefore may not be issued in accordance with *In re Goodman*, as cited above.

12. Claims 4, 6 and 21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 9, 17, 26 and 34 of U.S. Patent No. 6,295,209 B1 in view of Yunoki et al.

Application Claim 4 discloses that the notch is tapered from a surface of the layer toward the surface of the die. Patented Claims 9, 17, 26 and 34 do not teach this tapered feature of the notch. Yunoki et al. analogously teaches a circuit board device 30 for insertion into a connector 10 (Fig. 4), wherein the circuit board has a dielectric layer 34 with notches 35 located along the edge exposing circuit board terminals 32 (Fig. 2), said notches 35 being tapered (tapered portions shown at 35a) from a surface of the layer 34 toward the surface of the circuit board 30 in order to facilitate guiding the connector contacts 22 toward the exposed circuit board terminals 32 (Fig. 2; col.5: 63-col.6: 9). Since the analogous circuit board of Yunoki et al. and the semiconductor die of patented Claims 9, 17, 26 and 34 share the same structural features suitable for insertion into a connector body, as taught by Yunoki et al., then the use of tapered notches for facilitating insertion and reliable connection to the connector 10 of Yunoki et al. would have been readily recognized for use in the semiconductor die structure of patented Claims 9, 17, 26 and 34. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to taper the notches in patented Claims 9, 17, 26 and 34, as taught by Yunoki et al. and required by Application

Claim 4, in order to facilitate insertion and reliable connection to a connector, as taught by Yunoki et al.

Application Claims 6 and 21 disclose that the notch substantially surrounds the at least one corresponding bond pad. Claims 9, 17, 26 and 34 disclose that the notch exposes the bond pads through the polymer layer but do not teach the structural relationship between each notch and corresponding die bond claimed in Application Claim 6. Yunoki et al. analogously teaches a circuit board device 30 for insertion into a connector 10 (Fig. 4), wherein the circuit board has a dielectric layer 34 with notches 35 located along the edge that substantially surround the corresponding circuit board bond pads 32 in order to expose the bond pads 32 to the outside (Fig. 2), the dielectric layer 34 covering and inherently protecting the remaining portion of the connection surface 31 of circuit board 30 (col.5: 23-27). Since the analogous circuit board Yunoki et al. and the semiconductor die of Claims 9, 17, 26 and 34 both have a layer of insulating material for protection of the circuitry on the active surface, then substantially surrounding the bond pads with the notches in the insulating material, taught by Yunoki et al., would have been readily recognized in the art of patented Claims 9, 17, 26 and 34 in order to protect as much of the active surface circuitry as possible, exposing only the bond pads required for external contact. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the polymer notch structures in patented Claims 9, 17, 26 and 34 to substantially surround the at least one corresponding bond pad, as taught by Yunoki et al. and required by Application Claims 6 and 21, in order to maximize the protection of the active surface

circuitry of the semiconductor die, as taught in the analogous circuit board art of Yunoki et al.

13. Application Claims 5 and 18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 9, 17, 26 and 34 of U.S. Patent No. 6,295,209 B1 in view of Akram et al.

Patented Claims 9, 17, 26 and 34 teach all the elements of Application Claims 5 and 18 including that the polymer layer covers at least a portion of the active surface (the active surface, *generally*, in patented Claim 26; and the portion of the active surface *adjacent to* or *proximate* the semiconductor edge in patented Claims 9, 17 and 34). Patented Claims 9, 17, 26 and 34 do not teach that the polymer layer covers *substantially all* of the semiconductor active surface. Akram et al. teaches a semiconductor die 12 comprising a ceramic layer 20 (col.5: 47-51), the layer 20 having a notch 22 proximate the edge that exposes contact pads 116 (Figs. 6 and 7) and that covers all the remaining active die surface (i.e., covers "substantially all" of the active die surface) in order to protect the active surface circuitry from environmental contaminants. Since patented Claims 9, 17, 26 and 34 and Akram et al. are in the same art of mounting semiconductor die in electronic packages, then the protection of the active die surface would have been readily recognized in the pertinent art of patented Claims 9, 17, 26 and 34. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to protect the active surface circuitry by modifying the polymer layer in patented Claims 9, 17, 26 and 34 to cover

substantially all of the active surface except the bond pads, as taught by Akram et al., in order to ensure device reliability and longevity.

14. Application Claim 9 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 9, 17, 26 and 34 of U.S. Patent No. 6,295,209 B1 in view of Yunoki et al.

Application Claim 9 requires that the polymer layer includes regions extending laterally between adjacent bond pads of the at least some bond pads. Claims 9, 17, 26 and 34 disclose that the polymer layer has notches in the layer that expose the active surface bond pads but do not teach that the polymer layer includes regions extending laterally between adjacent bond pads of the at least some bond pads claimed in Application Claim 9. Yunoki et al. analogously teaches a circuit board device 30 for insertion into a connector 10 (Fig. 4), wherein the circuit board has a dielectric layer 34 with notches 35 located along the edge that substantially surround the corresponding circuit board bond pads 32 such that the layer includes regions extending laterally between adjacent bond pads 32 of at least some of the bond pads 32 (Fig. 2), said regions providing protection for the insertion portion of the active surface of the circuit board (col.5: 23-27). Since the analogous circuit board Yunoki et al. and the semiconductor active surface of Claims 9, 17, 26 and 34 both have a layer of insulating material for protection of the circuitry on the active surface, then providing regions of an insulating layer extending laterally between adjacent bond pads of at least some of the bond pads, as taught by Yunoki et al., would have been readily recognized in the art of patented Claims 9, 17, 26 and 34 in order to protect as much of the active surface

circuitry as possible and protecting the active surface proximate the edge when mounted. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the polymer layer in patented Claims 9, 17, 26 and 34 such that the layer includes regions extending laterally between adjacent bond pads of the at least some bond pads in order to protect as much of the active surface circuitry as possible, especially the active surface proximate the edge when mounted, as taught in the analogous circuit board art of Yunoki et al.

15. Claim 14 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 9, 17, 26 and 34 of U.S. Patent No. 6,295,209 B1 in view of Yunoki et al.

Application Claim 14 requires that at least one edge of the at least one notch is beveled. Patented Claims 9, 17, 26 and 34 do not teach this beveled feature of at least one edge of the at least one notch. Yunoki et al. analogously teaches a circuit board device 30 for insertion into a connector 10 (Fig. 4), wherein the circuit board has a dielectric layer 34 with notches 35 located along the edge exposing circuit board terminals 32 (Fig. 2), said notches 35 being beveled at the inner lateral edges of the notch (beveled portions shown at 35a) in order to facilitate guiding the connector contacts 22 toward the exposed circuit board terminals 32 (Fig. 2; col.5: 63-col.6: 9). Since the analogous circuit board of Yunoki et al. and the semiconductor die of patented Claims 9, 17, 26 and 34 share the same structural features suitable for insertion into a connector body, as taught by Yunoki et al., then the use of beveled notches for facilitating insertion and reliable connection to the connector 10 of Yunoki et al. would

have been readily recognized for use in the semiconductor die structure of patented Claims 9, 17, 26 and 34. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to bevel the notches in patented Claims 9, 17, 26 and 34, as taught by Yunoki et al. and required by Application Claim 14, in order to facilitate insertion and reliable connection to a connector, as taught by Yunoki et al.

16. It is clear that the Applicant has voluntarily exercised a choice to provide, in the instant Application, claims which represent genus claims already covered by the species claims that appear in the US Patents 6,144,560 and 6,295,209 B1, respectively, and claims which are obvious thereover in view of prior art. The grant of an extension of the right to exclude the public from making and/or using the invention for longer than the statutory life of the reference patents cannot be justified. However, **the Applicant may overcome the above patenting rejections by submitting terminal disclaimers in accordance with 37 CFR § 1.321(c)(1)-(3)**.

17. In summary, Claims 1, 4-9, 11, 12, 14 and 16-21 have been rejected in the obviousness-type Double Patenting rejections, above.

Rejections Based On Prior Art

18. The following references were relied upon for the rejections hereinbelow:

Lee et al. (US 5,386,087)* Yunoki et al. (US 5,236,372)*

Dines (US 4,303,291)*

*Already of record in the instant Application.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1, 6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yunoki et al. in view of Dines and Lee et al.

As to Claim 1:

Ia. Yunoki et al. discloses at least one bond pad 32, 33 on a surface of circuit board 30 adjacent an edge 31 thereof; a layer 34 comprising dielectric material on at least a portion of the surface, the layer 34 having a notch 35 formed therein which exposes at least a portion of the at least one bond pad 32, 33 (col.5: 23-27).

Ib. Yunoki et al. does not indicate the functional circuitry or components on the circuit board or card 30.

Ic. However, Yunoki et al. discloses circuit boards or cards for mounting into system board connectors 10 for electronic devices (see Fig. 1; col.1: 6-15), and furthermore, cards such as SIMMs, DIMMs, controller cards, processor cards are notorious in the art as add-on circuit boards that have semiconductor chips mounted thereon for the above-mentioned memory, control, communication and processing functions to be provided on an electronic device or computer system board. Accordingly, these circuit cards are part of the *packaging* of the SIMMs, DIMMs,

controllers, communication devices and processors which are, respectively, representative of the various types of *semiconductor devices, i.e., circuit-board-packaged devices having semiconductor chips mounted thereon*, that are notorious in the art, as mentioned above.

Id. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit card 30 of Yunoki et al. to be a SIMM, DIMM, controller or processor card--i.e., a *semiconductor device* 30--for use in the electronic device contemplated by Yunoki et al.

IIa. Yunoki et al. teaches a dielectric (insulating) layer 34 for protecting the connector portion 31 of the semiconductor package circuit card 30 but is silent as to the dielectric material composition of the layer 34.

IIb. Dines teaches a circuit card with a dielectric layer 13 having notches 46 exposing bond pads 43, wherein the dielectric layer 13 is a photoimageable material which is developed and set by exposure to ultraviolet (UV) light (Fig. 2; col.3: 12-18 and 55-62).

IIc. Lee et al. further discloses that such a UV photoimageable layer is a photopolymer material which cross-links (sets) upon exposure to UV light (Fig. 1; col.3: 44-46).

IId. Since Yunoki et al. and Dines and Lee et al. all protect the circuit substrate with a planar member dielectric layer, and Yunoki et al. and Dines are both in the same art of attaching circuit cards to a system connector, and since Dines and Lee et al. teach a photoimageable polymer material for protecting the card surface, then the use

of the photoimageable polymer material for protecting the circuit card surface, as taught by Dines and Lee et al. would have been readily recognized as a an effective insulating material for the dielectric layer 34 in Yunoki et al.

IIe. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to specifically use the dielectric material taught by Dines and Lee et al. (i.e., the photoimageable polymer material) as the dielectric material 34 in Yunoki et al. in order to effectively apply a dielectric layer for protecting the connector portion 31 on the circuit card component 30 of the semiconductor package of Yunoki et al.

As to Claim 6, modified Yunoki et al. further discloses that notch 35 substantially surrounds at least one contact pad (i.e., contact pad 33: Fig 2).

As to Claim 7, modified Yunoki et al. further discloses a plurality of bond pads (i.e., pads 32 and 33: Fig. 2).

As to Claim 8, modified Yunoki et al. further discloses that at least some of the bond pads (i.e., pads 32) are located adjacent the edge (Fig. 2).

As to Claim 9, modified Yunoki et al. further discloses that layer 34 includes regions extending laterally between adjacent bond pads 32 of the at least some bond pads 32 (Fig. 2).

As to Claim 11, Yunoki, as modified by Dines and Lee et al. in parts IIa-e of the rejection of base Claim 1, above, teaches a photoimageable polymer material.

Response to Arguments

21. Applicant's amendments to the claims that include the combination of the notched "polymer" material and the "semiconductor die" have overcome the rejections over the prior art of record. The Examiner notes that amended Claim 1 was, evidently, inadvertently not amended to change "semiconductor device" to --semiconductor die-- in line 2 of the claim, said "semiconductor **die**" being clearly what was intended by the Applicant (see the paragraph of *Remarks* bridging pp.5-6 of Applicant's above-cited Amendment). This oversight necessitated the above rejection of Claims 1, 6-9 and 11 over Yunoki et al. in view of Dines and Lee et al. which applies to the semiconductor "device," as presently claimed. However, the above rejections may be overcome by changing "device" to --die-- in line 2 of base Claim 1.

Allowable Subject Matter

22. Claims 2 and 3 would be allowable if base Claim 1 is rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, and upon overcoming the obviousness-type Double Patenting rejection of base Claim 1, as set forth in this Office action.

23. Claim 13 is objected to as being dependent upon a rejected base claim (base Claim 12 is rejected under obviousness-type Double Patenting), but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. The following is a statement of reasons for the indication of allowable subject matter:

Upon changing "device" to --die-- in line 2 of base Claim 1, patentability of Claims 1-11 will then reside in the patentable subject matter of base Claim 1; i.e., patentability will reside in the combined assembly of the notched ***polymer*** layer on ***a semiconductor die***, in further combination with the other limitations of base Claim 1.

As to Claims 12-21, patentability resides in a substantially planar ***polymer*** member having the claimed relationship of notch structure to bond pads upon positioning the notched ***polymer*** layer over an active surface of ***the semiconductor die***, in combination with the other limitations of base Claim 12.

25. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

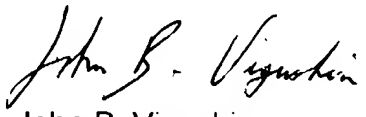
Park et al. (US 5,341,027) discloses a semiconductor die 31 with notches 36 in the semiconductor material exposing bonding pads 35 but does not teach a polymer layer positioned on the surface of die 31 and having notches for exposing bonding pads 35 of die 31.

Tanaka (JP61-187269 A) discloses a notched planar aluminum member 6 covering and thereby compensating for defects in film 4, the notches providing space for bonding wires 8 (Fig. 2 and English Abstract).

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



John B. Vigushin
Examiner
Art Unit 2827

jbv
May 6, 2003